Remarks/Arguments

ITEM 1

In response to the objection to the Abstract. Applicant herein provides an amended Abstract which Applicant asserts meets the USPTO requirements.

ITEM 3

Claim Rejections – 35 USC 102(e):

Claims 1-8 stand rejected under 35 U.S.C. §102(e) as being anticipated by Ishizuka et al. (US6771235).

Applicant first points out that claim 1 has been amended to include the additional feature of the charge having "been accumulated during a just preceding sequence of connection of another electrode of the second array." Support for this feature is on page 4, lines 27-31 and page 12, lines 11-19.

Applicant asserts that Ishizuka does not anticipate amended claim 1 and dependent claims 2-8.

Claim 1

Ishizuka discloses a device for displaying images comprising:

> an image display panel (11) comprising a first array (col. 6, line 54, cathodes lines B1-Bn) and a second array (col. 6, line 53, anodes lines A1-Am) of electrodes which serve an array of cells (col. 6, lines 51-58, "E(m,n) … arranged in matrix"), where each cell is powered between an electrode of the first array and an electrode of the second array effecting between them an intrinsic capacitor C_i (see Figs. 1, 10, and 14-15),

power supply means for generating a potential difference between two terminals, which is implicitly inferred by the current sources 23i (see col.7, lines 11-13 and col.8, lines 33-41), and

drive means (see Fig.9):

-adapted for successively connecting each electrode of the second array to one of the terminals of the power supply means (col.6, lines 62-67),

-adapted for, during each sequence of connection of an electrode of the second array, for simultaneously connecting one or more or even all the electrodes of the first array to the other terminal of the power supply means to power (i.e. to allow the cells to emit light) at least one of the cells linked both to the respective electrode of the second array and the respective electrode of the first array (col.7, lines 7-15).

In Ishizuka, during the sequence of connection of an electrode of the second array, according to col. 9, lines 20-27 , "one horizontal scanning period (i.e. sequence of connection) may include a short delay time" (see Fig.18) in which both the first and second switches (col. 9, lines 22- 24 and Fig. 14-15) are turned OFF between the "PWM signal ON period in which the first switch in the anode line drive circuit 14 is turned ON and the PWM signal OFF period in which no PWM signal is generated to turn the second switch ON."

One skilled in the art of driving electroluminescent display panels understands that, during this short "delay time," the only transfer of charges that may take place within cells linked to the same cathode line Bi (see fig. 14-15, electrode of the first array in columns) can only flow through the diode of the only-one EL element $E_{1,S}$ which is linked to the anode electrode B_S under scan (i.e. electrode of the second array in rows), because (1) this anode electrode B_S is connected to the ground through the switch 21_S and (2) the other anode electrodes B_1, B_2, ..., B_{n-1}, B_n are connected to the bias potential Vcc through the switches 21_1, 21_2, ..., 21_{n-1}, 21_n (see Figs. 14-15). Moreover, this transferred charge, if any, has been accumulated during the sequence of connection of the anode electrode B_S under scan, but has not been accumulated

during a just prior/preceding sequence of connection of another anode electrode B_{S-1}, as in amended claim 1.

Consequently, amended claim 1 is not anticipated by Ishizuka. As such reconsideration of claim 1 is respectfully requested.

Claim 2

Claim 2 which depends on claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by Ishizuka.

Because claim 2 includes the combination of features of claim 1 and claim 1 is not anticipated by Ishizuka, claim 2 is not anticipated by Ishizuka. As such reconsideration of claim 2 is respectfully requested.

Claim 3

Claim 3 which depends on amended claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by Ishizuka.

Claim 3 is directed to the following additional feature: each image to be displayed is divided into pixels or subpixels to which are allocated luminous intensity data, each cell of the panel being assigned to a pixel or subpixel of the images to be displayed, the device for displaying images comprises means of processing said data so as to be able, during each sequence of connection of an (row) electrode of the second array, to modulate the duration of connection t'_{a1} of each (column) electrode of the first array to said power supply means and to modulate the duration of said transfer of charge t'_{a2} of the intrinsic capacitors of the other cells linked to the same (column) electrode of the first array, as a function of the luminous intensity datum of the cell that has to be powered between this electrode of the first array and this electrode of the second array.

In Ishizuka, the "control PWM signal" allows the modulation of the duration of connection t'_{a1} of each electrode of the first array to the power supply means ... as a function of the luminous intensity datum of the cell that is to be powered, but Applicant is unable to find in Ishizuka evidence of the "control PWM signal" allowing the modulation of the duration of the

transfer of charge t'_{a2} of the intrinsic capacitors ... as a function of the luminous intensity datum of the cell that is to be powered, as claimed in the invention in claim 3.

For this reason and the fact that claim 3 further includes the combination of features of claim 1 which Applicant asserted above is not anticipated by Ishizuka, claim 3 is not anticipated by Ishizuka. As such reconsideration of claim 3 is respectfully requested.

Claim 4

Claim 4 which depends on claim 3 stands rejected under 35 U.S.C. 102(e) as being anticipated by Ishizuka. Applicant asserts that this claim is not anticipated by Ishizuka.

Claim 4 is directed to the adaptation of the drive means so that, during each sequence of connection of an (row) electrode of the second array, said connection of each (column) electrode of the first array to said power supply means is carried out, as appropriate, at the end of a sequence and said transfer of charges is carried out, as appropriate, at the start of a sequence.

Ishizuka (col.9. lines 20-27; Fig.18) discloses the short "delay time" takes place between the PWM signal ON period and the PWM signal OFF period (see Fig.18). If the "sequence" is defined, according to the wording of claim 1 and 4, as a sequence during which the switch 21_S is connected to the ground in order to allow the current source 23_1 to power the EL elements of the cathode line B_S ("sequence" being the whole scanning period), the PWM signal ON period is "at the start of a sequence," and the PWM signal OFF period is "at the end of a sequence." As the transfer of charge that is quoted in the office action, if any, would take place during the short "delay time," this transfer of charge does not take place "at the start of a sequence," as claimed in claim 4.

For this reason and the fact that claim 4 further includes the combination of features of claims 1 which Applicant asserted above is not anticipated by Ishizuka, claim 4 is not anticipated by Ishizuka. As such, reconsideration of claim 4 is respectfully requested.

Claims 5-8

Claims 5-8 each ultimately depend on claim 1 and stand rejected under 35 U.S.C. 102(e) as being anticipated by Ishizuka. However, because claims 5-8 include the features of claim 1, Applicant asserts that the claims 5-8 are also not anticipated by Ishizuka in light of the same

reasons advanced by Applicant for claim 1. As such, reconsideration of claims 5-8 is respectfully requested.

ITEM 5

Claim 9

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka in view of Aziz et al. (US 6,811.896).

Claim 9 depends on claim 8 and ultimately depends on amended claim 1.

Claim 9 is directed to a device for displaying images comprising:

- an image display panel comprising a first array (column - anodes X) and a second array (row - cathodes Y) of electrodes which serve an array of cells (11), where each cell (11) may be powered between an electrode (column - anode) of the first array and an electrode (row - cathode) of the second array effecting between them an intrinsic capacitor Ci (specification at page 9, lines 22-27 and page 10, lines 22-23).
- power supply means for generating a potential difference between two terminals (see, specification at page 9,lines 29-31),
- drive means :

adapted for successively connecting each (row) electrode of the second array to one of the terminals of the power supply means (specification at page 9, lines 33-38),

adapted for, during each sequence of connection of a (row) electrode of the second array, simultaneously connecting one or more or even all the (column) electrodes of the first array to the other terminal of the power supply means in order to power the cell(s) linked both to this (row) electrode of the second array and this/these (column) electrodes of the first array (specification at page 9, lines 33-38"),

adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as said cell to be powered (see, specification at page 11, lines 37-39, 11-14, page 17, lines 17-29), **wherein said charge has been accumulated during a just preceding sequence of connection**

of another electrode of the second array (specification at page 4, lines 27-31 and page 12, lines 11-19),

and

- an organic electroluminescent layer having a thickness of less than or equal to 0.2 µm.

Ishizuka discloses a device for displaying images comprising:

an image display panel (11) comprising a first array (col. 6, line 54 : cathodes lines B1-Bn) and a second array (col. 6, line 53 : anodes lines A1-Am) of electrodes which serve an array of cells (col. 6, lines 51-58: "E(m,n) ... arranged in matrix"), where each cell is powered between an electrode of the first array and an electrode of the second array effecting between them an intrinsic capacitor C_i (see Figs. 1, 10, and 14-15),

power supply means for generating a potential difference between two terminals, which is *implicitly inferred by the* current sources 23i (see col.7, lines 11-13 and col.8, lines 33-41), and

drive means (see Fig.9):

-adapted for successively connecting each electrode of the second array to one of the terminals of the power supply means (col.6, lines 62-67),

-adapted for, during each sequence of connection of an electrode of the second array, for simultaneously connecting one or more or even all the electrodes of the first array to the other terminal of the power supply means to power *(i.e. to allow the cells to emit light)* at least one of the cells linked both to the respective electrode of the second array and the respective electrode of the first array (col.7, lines 7-15).

In Ishizuka, during the sequence of connection of an electrode of the second array, according to col.9, lines 20-27 , "one horizontal scanning period (i.e. sequence of connection) may include a short delay time" (see Fig.18) in which both the first and second switches (col. 9, lines 22- 24 and Fig. 14-15) are turned OFF between the "PWM signal ON period in which the first switch in the anode line drive circuit 14 is turned ON and the PWM signal OFF period in which no PWM signal is generated to turn the second switch ON."

One skilled in the art of driving electroluminescent display panels understands that, during this short "delay time," the only transfer of charges that may take place within cells linked to the same cathode line Bi (see fig. 14-15, electrode of the first array in columns) can only flow through the diode of the only-one EL element $E_{1,S}$ which is linked to the anode electrode B_S under scan (i.e. electrode of the second array in rows), because (1) this anode electrode B_S is connected to the ground through the switch 21_S and (2) the other anode electrodes B_1, B_2, ..., B_{n-1}, B_n are connected to the bias potential Vcc through the switches 21_1, 21_2, ..., 21_{n-1}, 21_n (see Figs. 14-15). Moreover, this transferred charge, if any, has been accumulated during the sequence of connection of the anode electrode B_S under scan, but has not been accumulated during a just prior/preceding sequence of connection of another anode electrode B_{S-1}, as in amended claim 9.

Aziz discloses "the luminescent region between the anode and cathode electrodes of the OLED" to be "usually less than 200 nm thick." (col. 1, line 56-58)

However, Ishizuka and Aziz separately and in combination fail to disclose a drive means that is "adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as said cell to be powered" in combination with the added feature of "said charge has been accumulated during a just preceding sequence of connection of another electrode of the second array" which is a key combination of the invention and generally recited in each of applicant's claims.

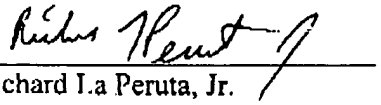
Therefore, current claim 9 is not made obvious by Ishizuka in view of Aziz. As such, reconsideration of the rejection to current claim 9 is requested.

Conclusion

In light of the above assertions and claim amendments, reconsideration of the rejections to each of the claims is respectfully requested.

If the Examiner has any questions or comments that would facilitate the disposition or resolution of the issues, he is respectfully requested to contact the undersigned at 609-734-6816.

Respectfully submitted,
Jean-Paul Dagois, Applicant



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